ABSTRACT OF THE DISCLOSURE

A system and method for effectuating the transfer of data blocks having intervals across a clock boundary between a first clock domain and a second clock domain. A first circuit portion provides the data blocks to a second circuit portion. A synchronizer controller disposed between the first and second clock domains provides at least one dead cycle control signal to the second circuit portion, which is indicative of the location of at least one dead cycle between the first and second clock signals. Control logic associated with the second circuit portion generates data transfer control signals responsive to the at least one dead cycle control signal in order to control the second circuit portion so that the data blocks may be transmitted as contiguous data blocks relative to the at least one dead cycle.